SPECIFICATION AMENDMENTS

Replace the paragraph beginning on page 5, line 23 with the following paragraph:

Turning now to the drawings, Fig 1 is a block diagram of a vehicle detector system incorporating the invention. As seen in this Fig., the vehicle detector system includes a pair of vehicle detectors with synchronous intercoupling. A first vehicle detector 10 designated with the legend "MASTER" [[has]] having an oscillator 12 operable over a frequency range of about 10 to about 120 kHz is coupled via a transformer 13 to an inductive loop 14. Inductive loop 14 is typically mounted within the roadbed in a position such that vehicles to be sensed will pass over the loop. Such loops are well-known and are normally found installed at controlled locations in the highway system, such as at intersections having signal heads controlled by a local intersection unit, parking lots with controlled access, railroad crossings, security barrier installations and the like. Loop 14 may also be mounted adjacent a track switch in a railway system.

Replace the paragraph beginning on page 6, line 9 with the following paragraph:

Control unit 20 includes a second oscillator circuit which typically generates a precise, crystal controlled, relatively high frequency clock signal (*e.g.*, a 6 mHz clock signal). This high frequency clock signal is coupled via a second squaring circuit to a second binary counter, both of which are also included in control unit 20. The second binary counter is typically a multi-stage counter having a control input for receiving control signals generated within control unit 20 and a count state output for generating signals representative of the count state of the second binary counter at any given time. The count state of the second binary counter is coupled as one input to an arithmetic logic unit included within control unit 20. The other input to the arithmetic logic unit is one or more reference values stored in a reference memory within control unit 20.

The reference memory is controlled by appropriate signals generated within control unit 20 in the manner described below.

Replace the paragraph beginning on page 6, line 23 with the following paragraph:

An input/output unit 30 is coupled between the control unit 20 and a loop control unit 22, and externally associated circuitry via control signal path 31. I/O unit 30 accepts appropriate control signals via signal path 31 to specify the control parameters for the vehicle detector unit of Fig. 1, such as mode, sensitivity, and any special features desired. I/O unit 30 furnishes data output signals via signal path 31, the data output signals typically comprising Call signals indicating the arrival or departure of a vehicle from the vicinity of the associated loop and other display signals. Loop control unit 22 controls the direct operation of oscillator 12.

Replace the paragraph beginning on page 8, line 9 with the following paragraph:

A second vehicle detector 10' designated with the legend "SLAVE" is comprised of the same functional elements as MASTER detector 10. The functional elements of SLAVE detector 10' are designated with the same numerals using a prime symbol'. SLAVE detector 10' functions in the same manner as MASTER detector 10 for vehicle detection purposes, with the exception that MASTER detector 10 controls the synchronization of the system in the manner described below.

Replace the paragraph beginning on page 9, line 18 with the following paragraph:

In the series synchronization implementation illustrated in Fig. 2, only one channel from all the channels in the detector system is active at any given time. The sampling process begins with master detector #1 sampling all its channels one by one. When finished, the master detector sends a Synch Out pulse to detector #2 which signals detector #2 to begin sampling its channels. When detector #2 has finished sampling all its channels, it sends a Synch Out [[pulst]] pulse to detector #3 which signals detector #3 to begin sampling all its channels. When the last detector in the series has finished sampling all its channels, it sends a Synch Out pulse to the master detector, which then starts to sample all its channels. Fig. 3 shows the interrelationship between the timing of the Master Synch Out pulse, the commencement of slave sampling, and the re-commencement of master sampling. For clarity, Fig. 3 is limited to the one MASTER- one SLAVE configuration shown in Fig. 1. The extension to one MASTER-three SLAVES configuration will be obvious to one of ordinary skill in the art.

Replace the paragraph beginning on page 10, line 18 with the following paragraph:

The following is a summary of the Series Synch Operation as performed by one MASTER and one or more SLAVES.

MASTER

Set Synch Duration Time to be 350ms

If Synch In=high; Else Goto (A)

Drive Synch Out low

Wait up to Synch Duration time for Synch In =low

(A)Drive Synch Out high, output 10ms pulse (tells slave to sample)

Start a Synch Duration Time timer, wait for Synch In=high (tells master to sample)

If the first complete loop has been done then set the Synch Duration Time to the loop time +15ms.

If it is after the Synch Duration Time has been determined, [[the]] then check the remaining time against the Synch Duration time, if it is not within + or – 15ms of Synch Duration time, then the synch had failed.
Glitch Pulse Test (verify Synch In=high for 1ms)
Set Start Sample flag
Drive Synch Out low
Start 15ms Timer
Wait for Synch In=low
Wait for Sample Done flag
Goto(A)

Replace the paragraph beginning on page 11, line 10 with the following paragraph:

Series Synch Failure

If Synch failed, then start a 600ms timer, then go back to synch and start from the beginning. If the error is corrected within 600ms, then the error is cancelled. If the error persists after 600ms, then the error is latched until a power down reset or a reset pin reset. Changing Synch Mode resets failure.

Replace the paragraph beginning on page 11, line 17 with the following paragraph:

Fig. 4 is a schematic diagram illustrating a vehicle detector system in a parallel synchronization configuration. As seen in this Fig., the Synch Out signal from detector #1 (the master detector) is connected to the Synch In signal inputs of detectors #2, 3, and 4 (all the slave detectors). The Synch Out signals from each of detectors #2, 3, and 4 (all the slave detectors) are all coupled in parallel to the Synch In signal input of detector #1 (the master detector).

Replace the section beginning on page 12, line 9 with the following section:

5. If the next sampling channel is the last channel (channel 4), then continue to 6. If the next sampling channel is not the last channel (c[[g]]hannel 4), set the Synch Out low after 5ms.